REMARKS

Claims 34 and 37-48 are pending. Claims 1-33, 35 and 36 are cancelled. New claims 44-48 are added.

REJECTION UNDER 35 U.S.C. 102

Claims 34 and 37-42 stand rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici.

Dependent claim 43 stand rejected under 35 U.S.C. 103 as being unpatentable over Abramovici in view of Mansingh.

Claim 34 has been amended to clarify the claimed language.

Claim 34, as amended, recites a processing device, comprising:

-a reconfigurable circuit allowing change in function and connection relation;

-a setting portion storing setting data representing a divided unit forming a part of an intended circuit, and supplying the setting data to said reconfigurable circuit; and

-a control portion controlling said setting portion such that a plurality of setting data are successively supplied to said reconfigurable circuit to configure said intended circuit.

The claim specifies that:

-said reconfigurable circuit has N state holding circuits holding an internal state;

-said reconfigurable circuit is divided, by an arrangement of said N state holding circuits, into (N+1) stages of reconfigurable units;

-said control portion controls said setting portion such that, when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow,

-said control portion controls said setting portion such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to the reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit,

-said control portion controls said setting portion such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to the reconfigurable unit between the (i+1)th state holding circuit and (i+2)th state holding circuit in accordance with the process flow, and

-said control portion controls said setting portion such that at said next time point, setting data of a divided unit configuring a different intended circuit is supplied to the reconfigurable unit between the i-th state holding circuit and the (i+1) state holding circuit.

Considering the reference, the technique of Abramovici is directed to assigning a plurality of processes successively to a reconfigurable circuit for sequential processing thereof.

Namely, Abramovici teaches processing with a plurality of processes assigned sequentially to a reconfigurable circuit.

In contrast, according to claim 34, a plurality of processes are carried out in parallel. Specifically, the claim recites that:

(a) the control portion controls said setting portion such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to the reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit,

(b) the control portion controls said setting portion such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to the reconfigurable unit between the (i+1)th state holding circuit and (i+2)th state holding circuit in accordance with the process flow, and

(c) the control portion controls said setting portion such that at said next time point, setting data of a divided unit configuring a different intended circuit is supplied to the reconfigurable unit between the i-th state holding circuit and the (i+1)th state holding circuit.

For example, as shown in Fig. 30, the setting data of divided unit FA5 (that may correspond to "the divided unit configuring an intended circuit" in the claimed feature (a) presented above) is supplied to the second stage that may correspond to "the reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit" in the claimed feature (a), at the fifth cycle that may correspond to "one time point" in the claimed feature (a).

At the next, sixth cycle that may correspond to "next time point" in the claimed feature (b) presented above, the setting data of divided unit FA6 that may correspond to "a next divided unit configuring said intended circuit" in the claimed feature (b), is supplied to the third stage that may correspond to "the reconfigurable unit between the (i+1)th state holding circuit and (i+2)th state holding circuit" in the feature (b).

At this sixth cycle ("said next time point" in the feature (c) presented above), the setting data of divided unit FB5 that may correspond to " a divided unit configuring a different intended circuit" in the feature (c) is supplied to the second stage that may correspond to " the reconfigurable unit between the i-th state holding circuit and (i+1)th state holding circuit" in the feature (c).

Thus, the features (a), (b) and (c) of claim 34 discussed above make it possible to carry out a plurality of processes, such as function A (FA) and function B (FB), in parallel.

Abramovici does not disclose the claimed features (a), (b) and (c).

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference.

Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

As demonstrated above, Abramovici neither expressly not inherently discloses the claimed features (a), (b) and (c) discussed above. Hence, claim 34, as amended, is not anticipated by Abramovici.

Moreover, as demonstrated above, the reference does not suggest carrying out a plurality of processes in parallel. Therefore, the claimed features (a), (b) and (c) are not obvious over Abramovici.

Claims 37-43 dependent from claim 34 are defined over the prior art at least for the reasons presented above in connection with claim 34.

Newly added claims 44-48 further define the claimed invention.

In particular, independent claim 44 recites a processing device, comprising:

(a) a reconfigurable circuit capable of arranging a circuit that can be divided into at least three divided circuits successively on a same region in an order of a first divided circuit, a second divided circuit, and a third divided circuit;

(b) a memory portion storing an output of said reconfigurable circuit;

(c) a state holding portion operating faster than said memory portion, and storing an output of said reconfigurable circuit; and

(d) a switching portion selecting an output of said memory portion and an output of said state holding portion, and supplying the selected output to said reconfigurable circuit;

wherein

(e) said third divided circuit can be further divided into a fourth divided circuit and a fifth divided circuit, and allows arrangement successively on a same region in an order of said fourth divided circuit and said fifth divided circuit,

(f) when said fourth divided circuit is arranged on said reconfigurable circuit, said switching portion supplies an output of said first and second divided circuits stored in said memory portion to said reconfigurable circuit, and

(g) when said fifth divided circuit is arranged on said reconfigurable circuit, an output of said fourth divided circuit held in said state holding portion is supplied to said reconfigurable circuit.

For example, "first, second, and third divided circuits" may respectively correspond to FIR filter circuits 50, 52 and demodulating circuit 54 in Fig. 20.

Feature (e) is disclosed, for example, in Fig. 21. Specifically, the fourth divided circuit may be the circuit arranged on the reconfigurable circuit at the ninth cycle, and the fifth divided circuit may be the circuit arranged on the reconfigurable circuit at the tenth cycle.

Regarding feature (f), when the fourth divided circuit is arranged (e.g., "mov", "x", "sgn" on the first row; and "+", "mov" on the second row), MY#. MQ, and MI are input to the fourth divided circuit.

As clear from Fig. 20, MQ is the output from the second divided circuit (FIR filter circuit 52). MI is the output from the first divided circuit (FIR filter circuit 50).

The claimed recitation "supplies an output of said first and second divided circuits stored in said memory portion to said reconfigurable circuit" is disclosed, for example, in the paragraph starting from line 20 on page 22 that discloses that output signal MI is stored in a prescribed

area of memory portion 27, and in the paragraph starting from line 28 on page 22 that discloses that output signal MQ is stored in a prescribed area of memory portion 27.

With regards to feature (g), when the fifth divided circuit is arranged (e.g., "mov", "»1", "mov" on the first row; and "mov", "mov", "mov" on the second row), the output of the ninth cycle (fourth divided circuit) is input to the fifth divided circuit. It is noted that Fig. 21 includes the block of "HOLD RESULT OF PROCESSING" between the ninth cycle and the tenth cycle. Likewise with the example shown in Fig. 12 and Fig. 6, this means that data is held in internal state circuit 20 (that may correspond to state holding portion). This arrangement supports the claimed recitation "an output of said fourth divided circuit held in said state holding portion is supplied to said reconfigurable circuit".

It is respectfully submitted that the prior art of record does not teach or suggest the arrangement of claim 44. For example, Abramovici does not teach or suggest that:

(e) said third divided circuit can be further divided into a fourth divided circuit and a fifth divided circuit, and allows arrangement successively on a same region in an order of said fourth divided circuit and said fifth divided circuit,

(f) when said fourth divided circuit is arranged on said reconfigurable circuit, said switching portion supplies an output of said first and second divided circuits stored in said memory portion to said reconfigurable circuit, and

(g) when said fifth divided circuit is arranged on said reconfigurable circuit, an output of said fourth divided circuit held in said state holding portion is supplied to said reconfigurable circuit.

The claimed features (e), (f) and (g) allow providing parallel processing employing a reconfigurable circuit having the divided circuits set forth above successively configured. For

example, operation by the FIR filter circuit that processes the I axis signal, and operation by the FIR filter circuit that processes the Q axis signal can be processed substantially in parallel.

In view of the foregoing, and in summary, claims 34 and 37-48 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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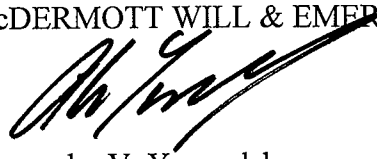

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